

#### FEATURES

- 8-Bit Resolution
- 20 MHz Sampling Rate
- DNL =  $\pm 1/2$  LSB, INL =  $\pm 1$  LSB (typ)
- Internal S/H Function
- Single Supply: 5 V
- $V_{IN}$  DC Range: 0 V to  $V_{DD}$
- $V_{REF}$  DC Range: 1 V to  $V_{DD}$
- Low Power: 85 mW typ. (excluding reference)
- Latch-Up Free
- ESD Protection: 2000 V Minimum

- Power Down Available: MP8776
- 3 V Version: MP87L75
- Small 20 Pin SOIC Package

#### APPLICATIONS

- Digital Color Copiers
- Cellular Telephones
- CCD s Based Systems
- Hardware Scanners
- Video Capture Boards

#### GENERAL DESCRIPTION

The MP8775 is an 8-bit Analog-to-Digital Converter in a small 20 pin SOIC package. Designed using an advanced 5 V CMOS process, this part offers excellent performance, low power consumption and latch-up free operation.

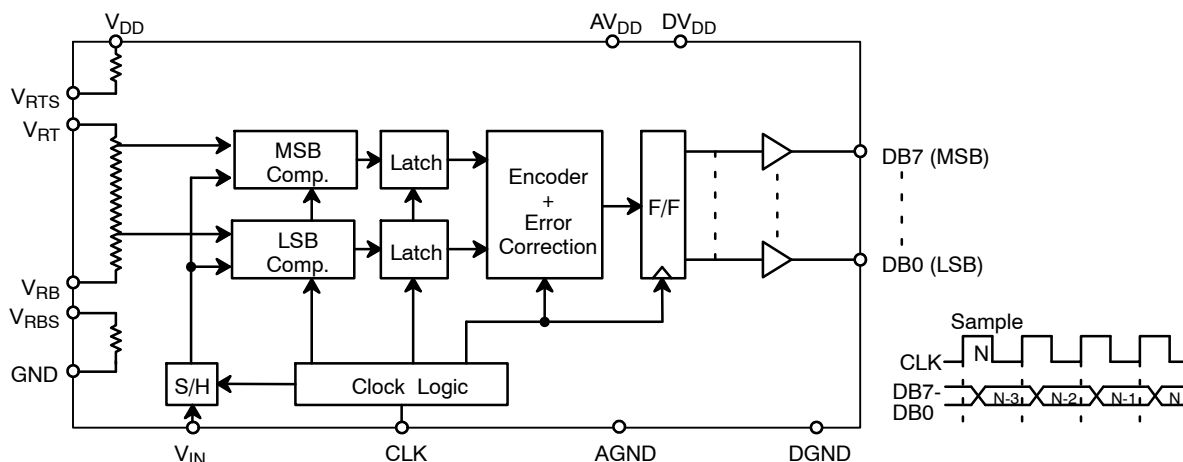
This device uses a two-step flash architecture to maintain low power consumption at high conversion rates. The input circuitry of the MP8775 includes an on-chip S/H function and allows the user to digitize analog input signals between GND and  $V_{DD}$ . Careful design and chip layout have achieved a low analog input capacitance. This reduces kickback and eases the requirements of the buffer/amplifier used to drive the MP8775.

The designer can choose the internally generated reference voltages by connecting  $V_{RB}$  to  $V_{RBS}$  and  $V_{RT}$  to  $V_{RTS}$ , or provide external reference voltages to the  $V_{RB}$  and  $V_{RT}$  pins. The internal reference generates 0.6 V at  $V_{RB}$  and 2.6 V at  $V_{RT}$ . Providing external reference voltages allows easy interface to any input signal range between GND and  $V_{DD}$ . This also allows the system to adjust these voltages to cancel zero scale and full scale errors, or to change the input range as needed.

The device operates from a single +5 V supply. Power consumption is 85 mW at  $F_s = 20$  MHz.

Specified for operation over the commercial / industrial ( $-40$  to  $+85^\circ\text{C}$ ) temperature range, the MP8775 is available in Surface Mount (SOIC), Shrunk Small Outline (SSOP) and Plastic dual-in-line (PDIP) packages.

#### SIMPLIFIED BLOCK AND TIMING DIAGRAM

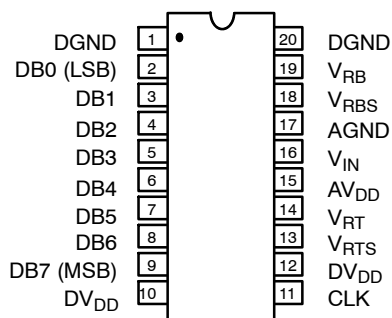


## ORDERING INFORMATION

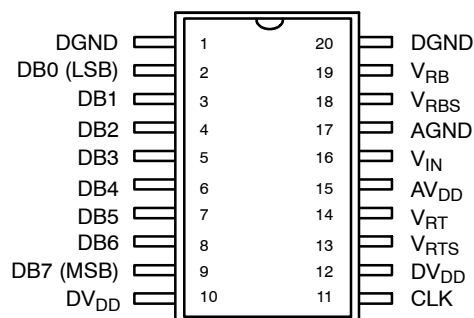
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
SOIC	-40 to +85°C	MP8775AS	±3/4	±1 1/2
PDIP	-40 to +85°C	MP8775AN	±3/4	±1 1/2
SSOP	-40 to +85°C	MP8775AQ	±3/4	±1 1/2

## PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



20 Pin PDIP (0.300 )



20 Pin SOIC (Jedec, 0.300 )  
20 Pin SSOP

## PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DGND	Digital Ground
2	DB0	Data Output Bit 0 (LSB)
3	DB1	Data Output Bit 1
4	DB2	Data Output Bit 2
5	DB3	Data Output Bit 3
6	DB4	Data Output Bit 4
7	DB5	Data Output Bit 5
8	DB6	Data Output Bit 6
9	DB7	Data Output Bit 7 (MSB)
10	DV <sub>DD</sub>	Digital Power Supply

PIN NO.	NAME	DESCRIPTION
11	CLK	Sample Clock
12	DV <sub>DD</sub>	Digital Power Supply
13	V <sub>RTS</sub>	Generates 2.6 V if tied to V <sub>RT</sub>
14	V <sub>RT</sub>	Top Reference
15	AV <sub>DD</sub>	Analog Power Supply
16	V <sub>IN</sub>	Analog Input
17	AGND	Analog Ground
18	V <sub>RBS</sub>	Generates 0.6 V if tied to V <sub>RB</sub>
19	V <sub>RB</sub>	Bottom Reference
20	DGND	Digital Ground

## ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified:  $AV_{DD} = DV_{DD} = 5\text{ V}$ ,  $FS = 15\text{ MHz}$  (50% Duty Cycle),  
 $V_{RT} = 2.6\text{ V}$ ,  $V_{RB} = 0.6\text{ V}$ ,  $T_A = 25^\circ\text{C}$

Parameter	Symbol	Min	25°C Typ	Max	Units	Test Conditions/Comments
<b>KEY FEATURES</b>						
Resolution		8			Bits	
Maximum Sampling Rate	FS	15	20		MHz	
<b>ACCURACY (A Grade)<sup>1</sup></b>						
Differential Non-Linearity	DNL			$\pm 3/4$	LSB	@ 15 MHz
Differential Non-Linearity	DNL			$\pm 1/2$	LSB	@ 10 MHz
Integral Non-Linearity	INL			1 1/2	LSB	Best Fit Line (Max INL - Min INL)/2
Zero Scale Error	EZS		$\pm 3$		LSB	
Full Scale Error	EFS		$\pm 3$		LSB	
<b>REFERENCE VOLTAGES</b>						
Positive Ref. Voltage	$V_{RT}$		2.6	$AV_{DD}$	V	$V_{REF} = V_{RT} - V_{RB}$
Negative Ref. Voltage	$V_{RB}$	AGND	0.6		V	
Differential Ref. Voltage <sup>3</sup>	$V_{REF}$	1.0		$AV_{DD}$	V	
Ladder Resistance	$R_L$	245	350	550	$\Omega$	
Ladder Temp. Coefficient	$R_{TCO}$		2000		ppm/°C	
Self Bias 1						
Short $V_{RB}$ and $V_{RBS}$	$V_{RB}$		0.6		V	
Short $V_{RT}$ and $V_{RTS}$	$V_{RT} - V_{RB}$		2		V	
Self Bias 2						
$V_{RB} = AGND_1$	$V_{RT}$		2.3		V	
Short $V_{RT}$ and $V_{RTS}$						
<b>ANALOG INPUT</b>						
Input Bandwidth (-1 dB) <sup>4</sup>	BW		50		MHz	
Input Voltage Range	$V_{IN}$	$V_{RB}$		$V_{RT}$	V	
Input Capacitance <sup>5</sup>	$C_{IN}$		16		pF	
Aperture Delay	$t_{AP}$		10		ns	
<b>DIGITAL INPUTS</b>						
Logical "1" Voltage	$V_{IH}$	4.0			V	$V_{IN} = DGND$ to $DV_{DD}$
Logical "0" Voltage	$V_{IL}$			1.0	V	
DC Leakage Currents <sup>6</sup>	$I_{IN}$				$\mu\text{A}$	
CLK			5		$\mu\text{A}$	
Input Capacitance			5		pF	
Clock Timing (See Figure 1.) <sup>7</sup>						
Clock Period	1/FS	50			ns	
High Pulse Width	$t_{PWH}$	25			ns	
Low Pulse Width	$t_{PWL}$	25			ns	
<b>DIGITAL OUTPUTS</b>						
Logical "1" Voltage	$V_{OH}$	4.5			V	$C_{OUT} = 15\text{ pF}$ $I_{LOAD} = 4\text{ mA}$ $I_{LOAD} = 4\text{ mA}$
Logical "0" Voltage	$V_{OL}$			0.4	V	
Data Valid Delay <sup>2, 8</sup>	$t_{DL}$		20	25	ns	
Data Hold Time	$t_{HL}$		12	15	ns	

## ELECTRICAL CHARACTERISTICS TABLE (CONT D)

Description	Symbol	Min	25°C Typ	Max	Units	Conditions
<b>AC PARAMETERS</b>						
Differential Gain Error	$d_G$		2		%	FS = 4 x NTSC
Differential Phase Error	$d_{PH}$		1		°	FS = 4 x NTSC
<b>POWER SUPPLIES</b>						
Operating Voltage ( $AV_{DD}$ , $DV_{DD}$ ) <sup>9</sup>	$V_{DD}$		5		V	
Current ( $AV_{DD}$ + $DV_{DD}$ )	$I_{DD}$		17	25	mA	Does not include ref. current

**Notes:**

- 1 Tester measures code transitions by dithering the voltage of the analog input ( $V_{IN}$ ). The difference between the measured and the ideal code width ( $V_{REF}/256$ ) is the DNL error (Figure 2.). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (Figure 3.). Accuracy is a function of the sampling rate (FS).
- 2 Guaranteed. Not tested.
- 3 Specified values guarantee functionality. Refer to other parameters for accuracy.
- 4 -1 dB bandwidth is a measure of performance of the A/D input stage (S/H + amplifier). Refer to other parameters for accuracy within the specified bandwidth.
- 5 See  $V_{IN}$  input equivalent circuit (Figure 4.). Switched capacitor analog input requires driver with low output resistance.
- 6 All inputs have diodes to  $DV_{DD}$  and  $DGND$ . Input DC currents will not exceed specified limits for any input voltage between  $DGND$  and  $DV_{DD}$ .
- 7  $t_R$ ,  $t_F$  should be limited to >5 ns for best results.
- 8 Depends on the RC load connected to the output pin.
- 9  $AGND$  and  $DGND$  pins are connected through the silicon substrate. Connect together at the package and to the analog ground plane.

Specifications are subject to change without notice

## ABSOLUTE MAXIMUM RATINGS ( $T_A = +25^\circ\text{C}$ unless otherwise noted)<sup>1, 2, 3</sup>

$V_{DD}$ to GND	7 V	Storage Temperature	-65 to +150°C
$V_{RT}$ & $V_{RB}$	$V_{DD} + 0.5$ to GND -0.5 V	Lead Temperature (Soldering 10 seconds)	+300°C
$V_{IN}$	$V_{DD} + 0.5$ to GND -0.5 V	Package Power Dissipation Rating @ 75°C	
All Inputs	$V_{DD} + 0.5$ to GND -0.5 V	SOIC, SSOP, PDIP	700 mW
All Outputs	$V_{DD} + 0.5$ to GND -0.5 V	Derates above 75°C	9 mW/°C

**Notes:**

- 1 Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
- 2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. All inputs have protection diodes which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
- 3  $V_{DD}$  refers to  $AV_{DD}$  and  $DV_{DD}$ . GND refers to  $AGND$  and  $DGND$ .

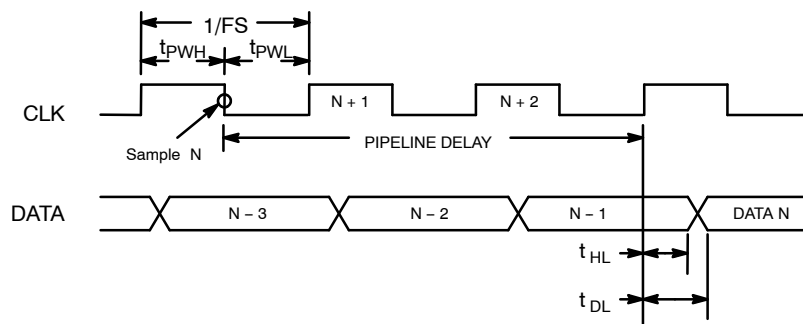


Figure 1. MP8775 Timing Diagram

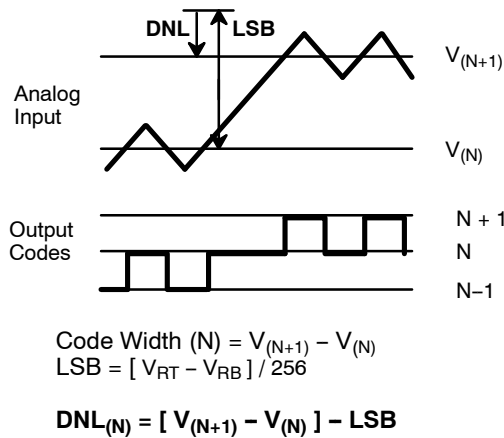


Figure 2. DNL Measurement

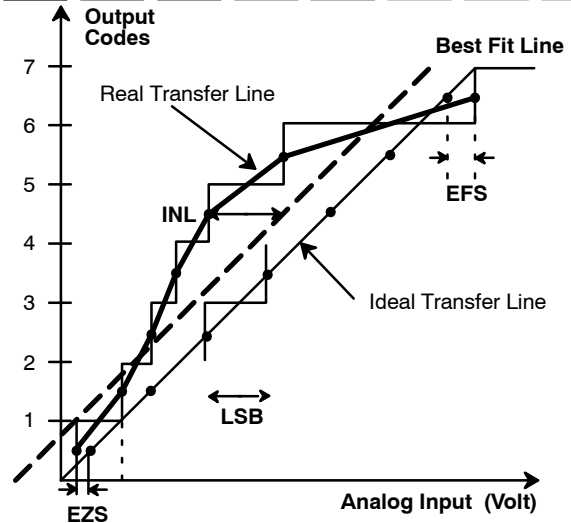


Figure 3. INL Error Calculation

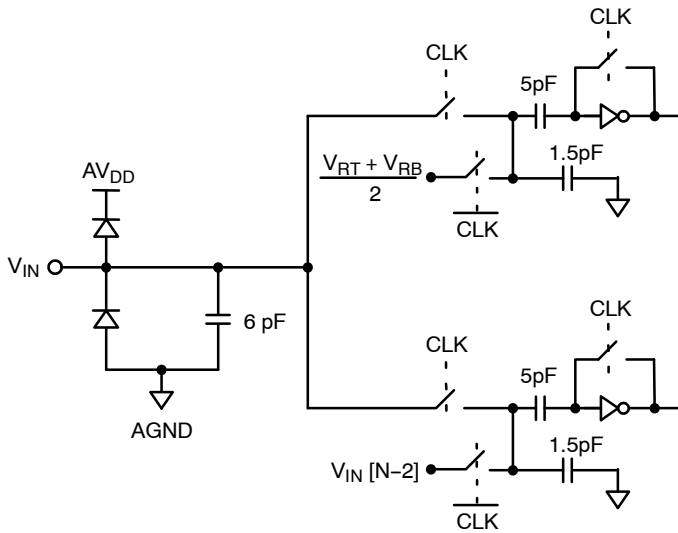


Figure 4. Equivalent Input Circuit

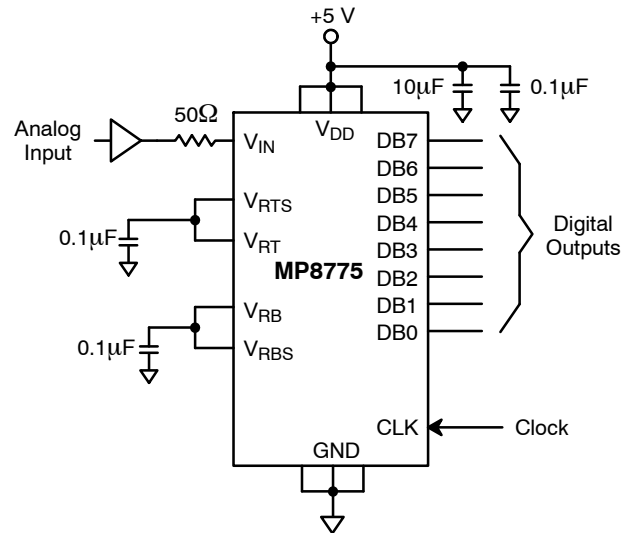


Figure 5. Typical Circuit Connections

**APPLICATION NOTES**

Signals should not exceed  $AV_{DD} + 0.5V$  or go below  $AGND - 0.5V$  or  $DV_{DD} + 0.5V$  or  $DGND - 0.5V$ . All pins have internal protection diodes that will protect them from short transients ( $< 100\mu s$ ) outside the supply range.

$AGND$  and  $DGND$  pins are connected internally through the P-substrate. DC voltage differences between these pins will cause undesirable internal substrate currents.

The power supply ( $AV_{DD}$ ) and reference voltage ( $V_{RT}$  &  $V_{RB}$ ) pins should be decoupled with  $0.1\mu F$  and  $10\mu F$  capacitors to  $AGND$ , placed as close to the chip as possible.

The digital outputs should not drive long wires or buses. The

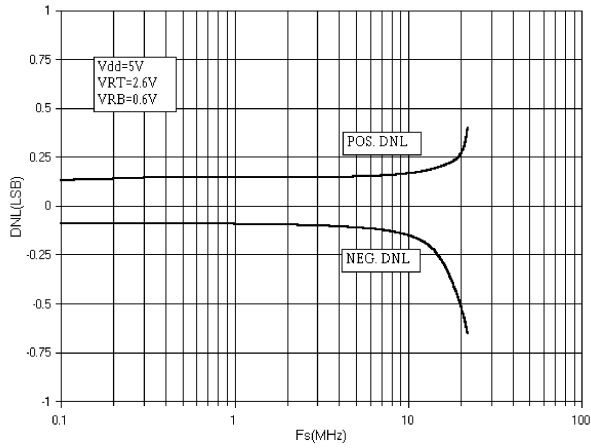
capacitive coupling and reflections will contribute noise to the conversion.

It is possible for the data valid delay ( $t_{DL}$ ) to be equal to or greater than the high pulse width of the sampling clock ( $t_{PWH}$ ). See Figure 1. This can cause timing related errors. For sample rates above 14 MSPS use only the rising edge of the sample clock (CLK) to latch data from the MP8775 to other parts of the system.

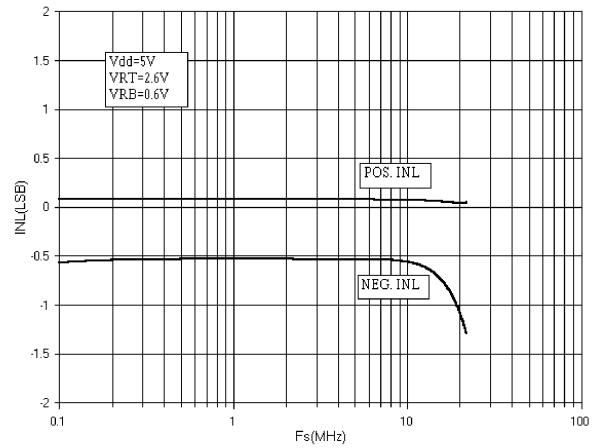
The reference can be biased internally by shorting  $V_{RT}$  to  $V_{RTS}$  and  $V_{RB}$  to  $V_{RBS}$ . This will generate  $0.6V$  at  $V_{RB}$  and  $2.6V$  at  $V_{RT}$  (see Figure 5).

If the internal reference pins  $V_{RTS}$  and/or  $V_{RBS}$  are not used they should be left unconnected.

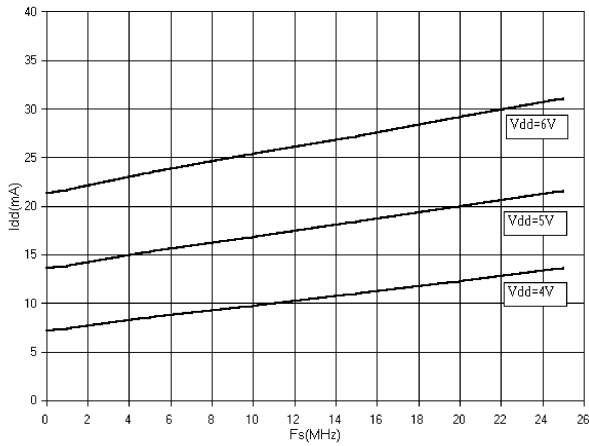
## PERFORMANCE CHARACTERISTICS



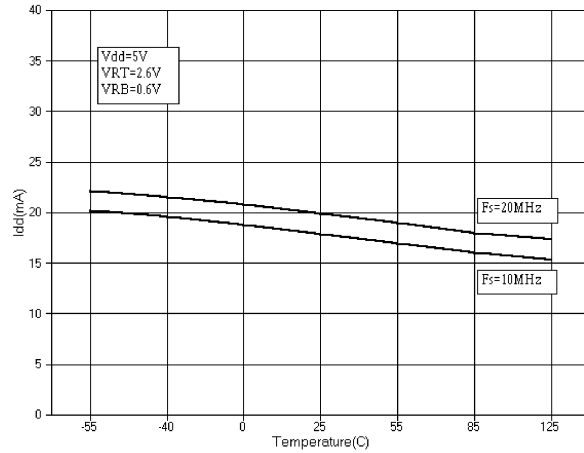
**Graph 1. DNL vs. Sampling Frequency**



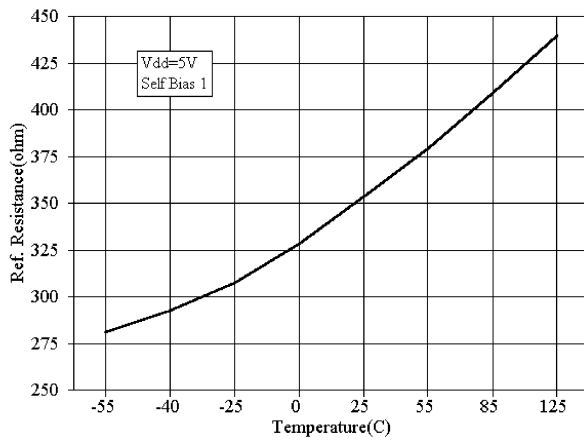
**Graph 2. INL vs. Sampling Frequency**



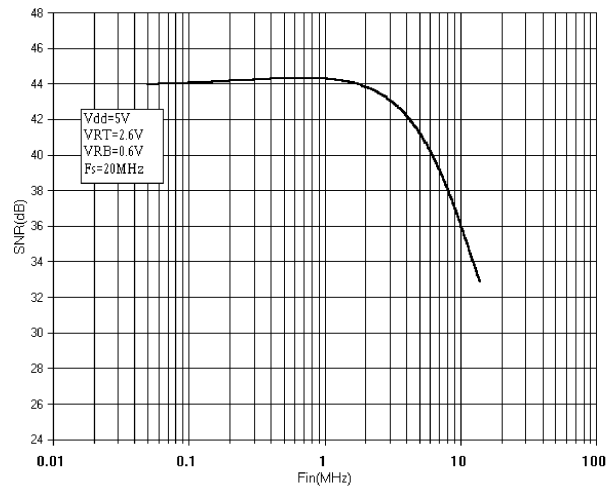
**Graph 3. Supply Current vs. Sampling Frequency**



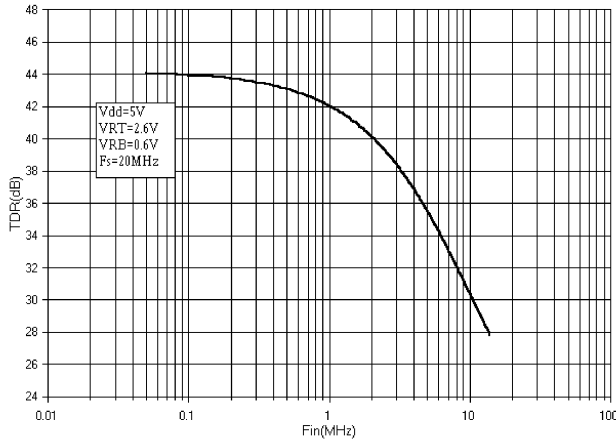
**Graph 4. Supply Current vs. Temperature**



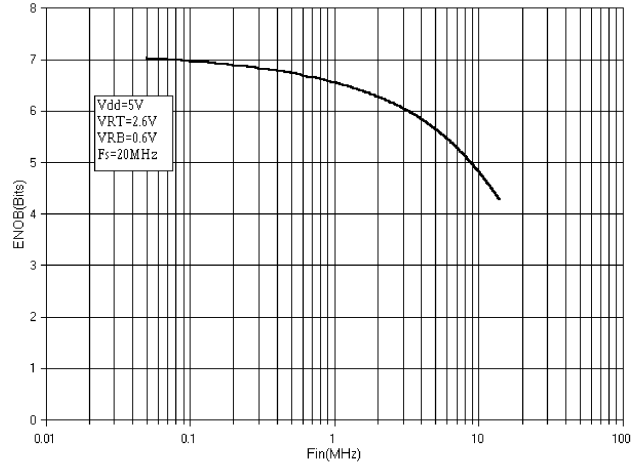
**Graph 5. Reference Resistance vs. Temperature**



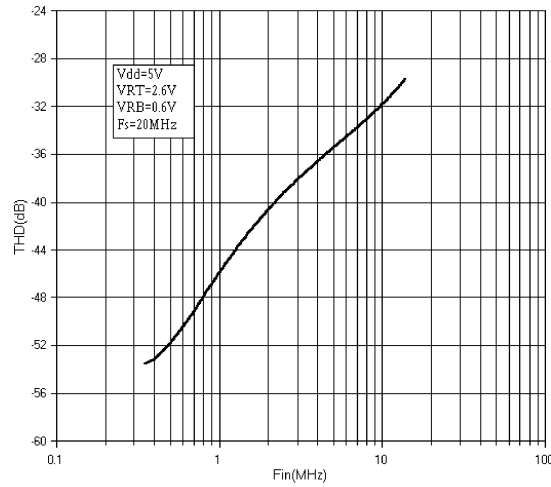
**Graph 6. SNR vs. Input Frequency**



**Graph 7. SINAD vs. Input Frequency**



**Graph 8. ENOB vs. Input Frequency**



**Graph 9. THD vs. Input Frequency**

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